

ELECTRONOTES

S-019

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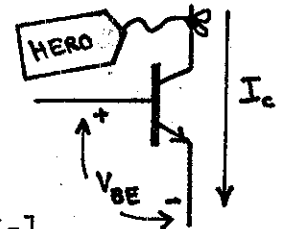
LOG AND EXPONENTIAL (ANTILOG) CIRCUITS

-by Bernie Hutchins

- ▷ The more or less ordinary bipolar junction transistor is the heart of most analog circuits that perform a logarithmic or anti-logarithmic conversion process. The property of the BJT that makes this possible is the exponential relationship between the collector current and the base-to-emitter voltage.

$$I_C = I' e^{qV_{BE}/kBT} \quad (1)$$

Fig. 1



Notes and Assumptions:

The BJT is high β [implying that $I_B = 0$, and $I_C = I_E$]

V_{BE} is much greater than $kBT/q = 26$ mV, with:

k_B = Boltzmann's constant

q = electron charge

T = absolute temperature (300° at room temperature)

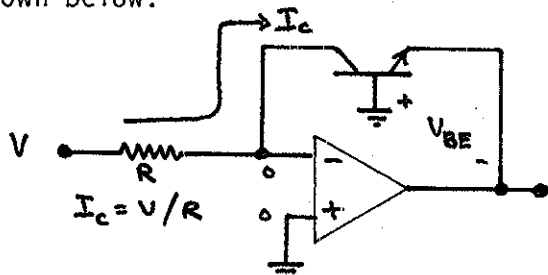
I' is the "reverse saturation current" $\sim 10^{-12}$ amps

This relationship is valid over a range of at least 10^6 and perhaps as far as 10^9 for some devices. It is an extremely useful relationship that would be difficult to generate any other way. Observe that if we wanted to control current over a 10^6 range with voltage with something linear (like a resistor), we might start with 10 volts to give the maximum current (corresponding to 10^6), in which case, 10^5 would be 1 volt, 10^4 would be 100 mV, 10^3 would be 10 mV, 10^2 would be 1 mV, 10 would be 100 μ V, and 1 would be 10 μ V. Clearly this range of voltage would be difficult to maintain, since 10 μ V is down in the noise background, and even 1 mV is difficult to keep accurate relative to the usual circuit offsets. We can rewrite equation (1) with 26 mV for kBT/q , in which case, V_{BE} should be in mV

$$I_C = I' e^{V_{BE}/26} \quad (2)$$

Thus, I_C changes by a full decade (10:1) when V_{BE} changes by 60 mV, and I_C changes by an octave (2:1) when V_{BE} changes by 18 mV.

- ▷ A number of simple one-transistor one op-amp circuits can then be designed as shown below:



Log

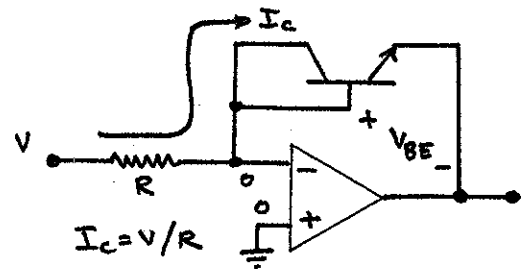
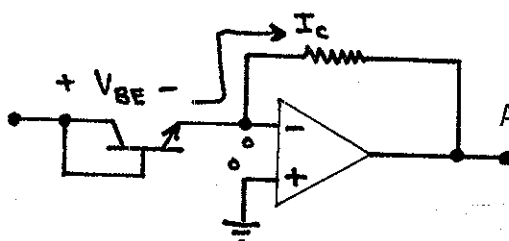
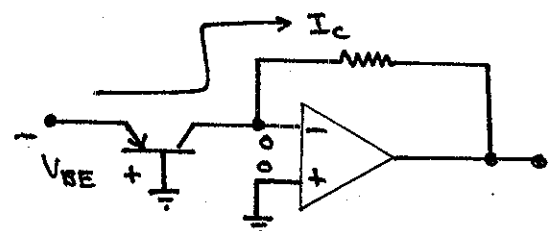


Fig. 2



Anti-Log



The circuits of Fig. 2, while instructive, have a very serious drawback. This is that the "reverse saturation current" I' is not well specified, and worse, it varies by a factor of two for each change of temperature by 10°C . This is about 7% per $^\circ\text{C}$ or somewhat over a musical half-tone. In addition, we should also keep in mind that what we are writing as 26 mV is really $k_B T/q$, and at room temperature of about 300°K , this exponential term causes a 0.33% change for each $^\circ\text{C}$ ($=^\circ\text{K}$). While this is small compared to 7%, it is still serious, and once the I' variation is corrected, we will need to attack this.

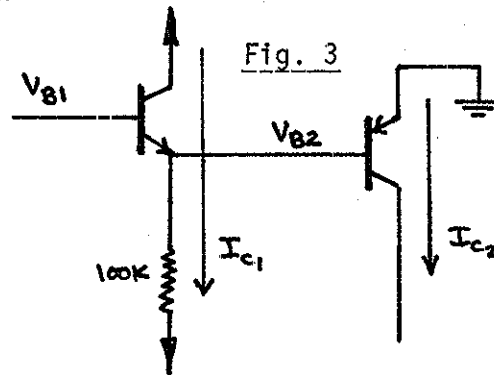
▷ The first means of correcting the I' factor is to use an emitter follower to drive the exponential converting transistor. The circuit is shown in Fig. 3, and involves an NPN transistor driving a PNP. Ideally, these would be a matched complimentary pair, but this is not very practical (matched monolithic pairs of the same type are very practical, and will be considered below). Thus we will not assume that both have the same reverse saturation current. Thus we use equation (2) to get:

$$I_{c1} = I'_1 e^{(V_{B1}-V_{B2})/26} \quad (3)$$

$$I_{c2} = I'_2 e^{-V_{B2}/26} \quad (4)$$

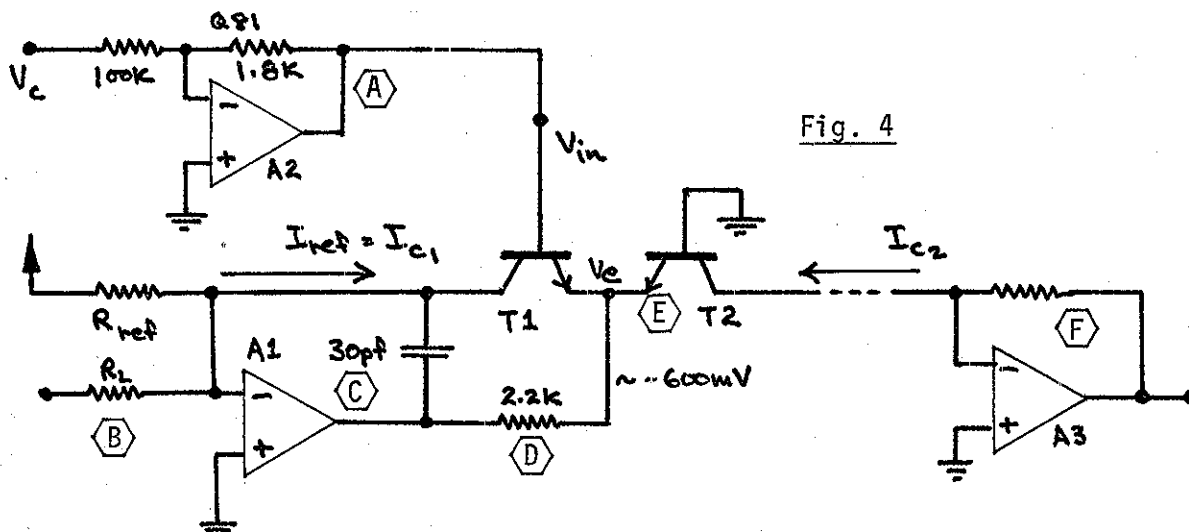
Note that the $-V_{B2}$ of equation (4) is the result of the fact that the transistor is PNP, not NPN. Combining (3) and (4), we arrive at:

$$I_{c2} = \frac{I'_2}{I'_1} I_{c1} e^{-V_{B1}/26} \quad (5)$$



If the two saturation currents I'_1 and I'_2 happened to be the same, this factor would disappear. This is difficult to achieve, but it is reasonable to assume that the ratio will track fairly well with temperature if the two transistors are glued together and sheltered from sudden temperature changes. $[V_{B1}]$ will usually be in the range of ± 180 mV (± 3 decades), and thus V_{B2} will be approximately 600 mV below V_{B1} , thus setting I_{c1} at about $(15 - 0.6)/100k$.

▷ A somewhat more elegant circuit is shown in Fig. 4, using a matched pair of NPN transistors and some op-amps:



In this circuit, an op-amp (A1) maintains a constant reference current ($=15/R_{ref}$) into the collector of T1, while the emitters are tied together. The equations for the two transistors are:

$$I_{c1} = I_{ref} = I' e^{(V_{in}-V_e)/26} \quad (6)$$

$$I_{c2} = I' e^{-V_e/26} \quad (7)$$

Combining, we get:

$$I_{c2} = I_{c1} e^{-V_{in}/26} = I_{c1} e^{-qV_{in}/kBT} \quad (8)$$

Thus, as before, we get rid of the I' dependence, here completely because we have assumed a matched monolithic pair for T1-T2. Additional points and/or features of the design are listed below as A, B, C, D, E, and F, corresponding to parts of the circuit in Fig. 4 with the corresponding letter in a hexigon.

- A. This op-amp inverter/attenuator serves three purposes.
1. It scales a standard 1 volt per octave control input V_C to the necessary 18 mV per octave needed at V_{in} .
 2. It inverts the control so that more positive voltages correspond to larger currents at I_{c2} .
 3. By using a Tel Labs type Q81 resistor with +3300ppm/°C (0.33%/°C), V_{in} is adjusted by a factor that exactly cancels the $1/T$ term of equation (8). Thus, in addition to I' compensation (the 7%), this circuit compensates the remaining 0.33%. The Q81 should be in thermal contact with the T1-T2 pair.
- B. I_{ref} is a standing current = $15/R_{ref}$, into the summing node of A1. From equation (8), we see that this is a linear factor of the current I_{c2} . By using a second voltage applied to R_L , a current corresponding to this voltage can be added or subtracted from the standing current, linearly modulating the output current.
- C. The added 30pf capacitor is needed to add additional compensation to op-amp A1. A1 is assumed to be unity-gain compensated, but the transistor in the feedback loop upsets this, and additional is needed.
- D. The reference current and I_{c2} are collected at the tied emitters and drawn out to the output of A1. The added 2.2k resistor serves to limit the current, since the output of A1 can go no lower than -15. Effectively, this sets an upper limit on I_{c2} .
- E. This circuit does not compensate for a bulk emitter resistance that is present, and effectively decreases the actual V_{BE} of T2 when the emitter current is large. This will be considered later.
- F. In many cases, we want to use the current I_{c2} directly. Where needed, a current-to-voltage converter A3 can be added.

The reader should understand that the improvements made in this circuit can also be made to additional circuits that follow.

▷ A simple rearrangement of the circuit elements of Fig. 4 convert the exponential circuit to a logarithmic one, as shown in Fig. 5:

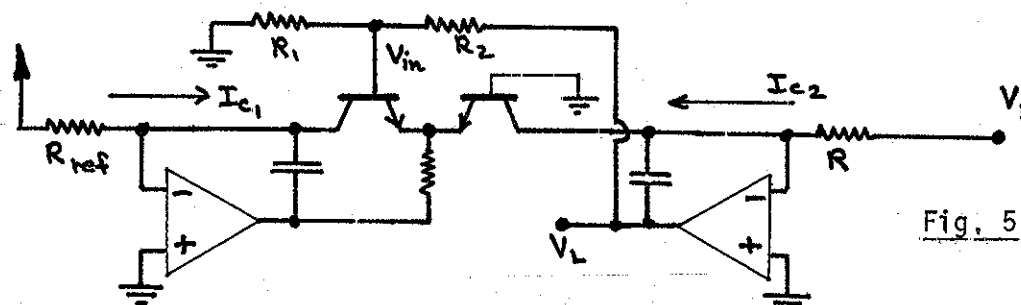


Fig. 5

While it is possible to analyze this log circuit starting with equation (1), we can just use equation (8). Here we will use volts instead of mV just for a change. Thus:

$$I_{c2} = I_{c1} e^{-V_{in}/0.026} \quad (9)$$

$$V_1/R = \frac{15}{R_{ref}} e^{-R_1 V_L/[0.026(R_1+R_2)]} \quad (10)$$

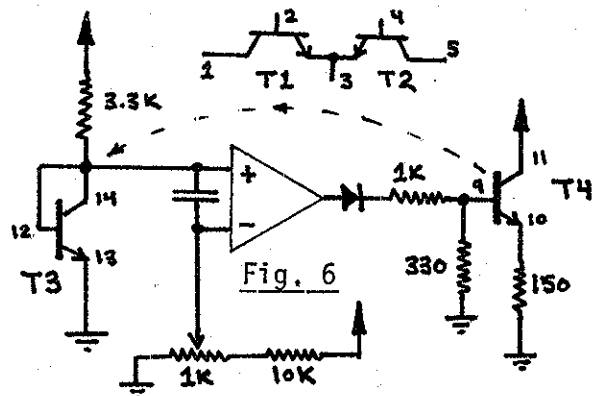
or:

$$V_L = \frac{-(R_1+R_2)}{R_1} (0.026) \ln \frac{R_{ref}}{15R} V_1 \quad (11)$$

Thus we have a working log circuit, and have seen how easily an exponential circuit can be converted to a log circuit.

▷ The ability to take logs and anti-logs can be a powerful technique when you consider that many operations can be performed simply in terms of logarithms. Note also that the 15 in equation (11) is a power supply voltage that determines I_{c1} , but it is only the current that is important, and 15 can be replaced with any arbitrary positive voltage. Thus equation (11) can be considered to indicate that Fig. 5 is capable of taking a log of a ratio. Furthermore, we can manipulate the log circuit in many ways. The R_1 - R_2 divider can be adjusted for a needed log base. We can further manipulate V_L before feeding to an anti-log circuit. If we double it, we get a squaring circuit from the anti-log, and if we divide V_L by two, we get a square root, and in a similar way, we can have any value of power or root needed. Also, the 15 volt supply that supplies the reference current in the anti-log circuit can also be an arbitrary positive voltage, giving us the ability to multiply a final result (of raising a ratio to a power) by another voltage. Thus a function of the form $Z(X/Y)^n$ can be realized. An added advantage is that when we take a log and then an anti-log, the 0.33% temperature dependence cancels out of the final result, and you save one or two of the temperature compensating Q81 resistors.

▷ Another form of temperature control is the method of thermostating the transistor pair (in theory all our problems go away if we hold the temperature constant, but it is well to still use the pair to get rid of I' dependence and rely on thermostating to just get rid of the 0.33%/°C term). One of the few practical ways of controlling the temperature of the pair is to use a monolithic transistor array. Two of the transistors on the array are used for the log or exponential function. Two of the remaining transistors are used for the temperature controller, one being a heater, and the other being the temperature sensor. A typical circuit assuming a type CA3046 NPN array is shown in Fig. 6. Here the matched, emitter-coupled pair on pins 1 - 5 are used for the exponential or log conversion. T3 is used to monitor the temperature while T4 is a heater. The op-amp supplies base current to turn on T4 when the temperature drops below a level set by the reference. It may seem that the op-amp is acting as a comparator, turning on and off as the temperature rises and falls. Actually, something much more interesting occurs. A negative feedback loop around the op-amp, due to thermal feedback, is actually present, and this allows the heater to maintain temperature in a continuous manner. Response is surprisingly rapid. Of course, you don't use both temperature control and the Q81 at the same time - that defeats the purpose.



▷ Brief mention was made above of a problem related to the finite "bulk emitter" resistance of the B-E junction. We can think of this as an equivalent resistance r_e in series with the B-E junction, and this is typically around 10 ohms, but may be as low as 1 ohm for some superior transistors. This is mainly a problem with I_{C2} . The reference current I_{C1} is fixed at a small value, but I_{C2} can be larger and the $I_{C2}r_e$ drop across the B-E junction can be significant. Thus the imposed V_{BE} has to be shared between an actual V_{BE} and the voltage drop across r_e . The part that is dropped across r_e does not enter into equation (1), and the result is a lower current than desired. Thus the result is that the exponential current falls short of its desired value on the high end. Thus some form of high-end compensation is desirable, and a number of schemes have been devised. Fig. 7 shows a scheme due to Dave Rossum of E μ -Systems, shown here for PNP transistors, but it can be used for NPN transistors or for log converters by simple alterations as suggested above.

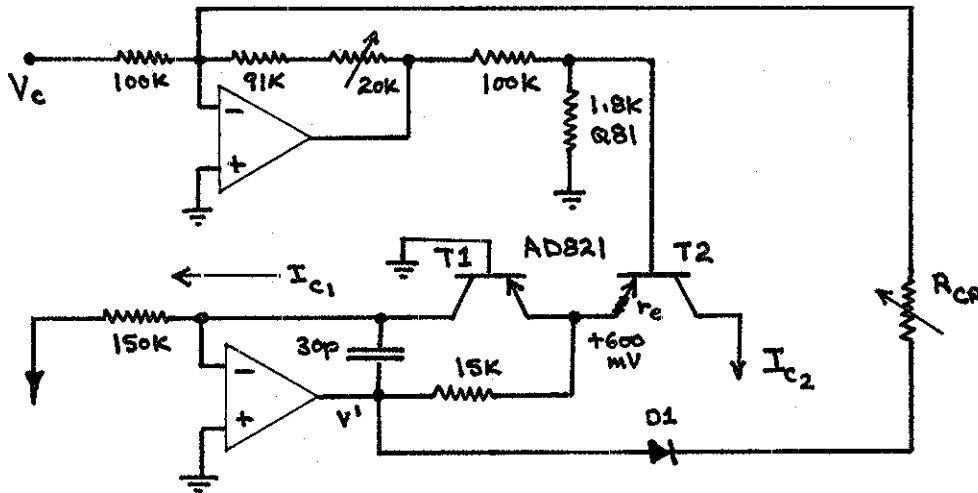
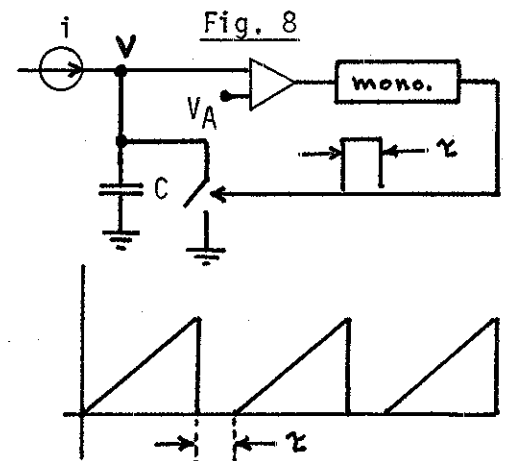


Fig. 7

In Fig. 7, the tied emitters are at a positive voltage of about +600 mV. As the current I_{C2} increases (and thus, the emitter current of T2), a voltage drop across r_e develops and a corresponding voltage drop across the 15k resistor also develops (we assume that for currents I_{C2} large enough to bother, I_{C1} can be ignored, although it also passes through the 15k resistor). Thus v' is about 600 mV plus $I_{C2} \cdot 15k$, while the bulk emitter resistance voltage drop is $I_{C2} \cdot r_e$. The diode D1 serves to cut out about the first 600 mV of v' , and thus a correction term proportional to the bulk emitter drop is available to be fed back to the control input through RCR.

▷ Many exponential current sources will be found with voltage-controlled oscillators. In addition to the bulk emitter resistance limiting the high end, a second factor is a finite reset or switching time that also causes the upper range to go flat. While due to separate causes, they are both of the same order. Therefore, it is a good idea to know about a simple compensation technique for reset time, as both can be useful, either in combination, or by having one do both jobs (overcompensating one will take care of the other).

A simple scheme for a sawtooth VCO is suggested in Fig. 8. A current source i charges a capacitor C . When the capacitor is charged to an amplitude controlling voltage V_A , a monostable is triggered which closes a switch for time τ , discharging the capacitor. For low frequencies, τ is not significant, but for high frequencies (see lower portion of Fig. 8), the finite reset time may cause the oscillator to go too far flat (lower than it's supposed to be).



A simple means of correcting this would be to cause the discharge to start early, before the ramp reaches V_A . The necessary conditions are derived as follows: The charging of the capacitor results in a ramp rate dV/dt of:

$$dV/dt = i/C \quad (12)$$

To reach an amplitude level V_A thus takes a time $V_A/(dV/dt)$, and the nominal frequency is the reciprocal of this time, or:

$$f = \frac{dV/dt}{V_A} \quad (13)$$

To cause the comparator to trigger early, we need to add to V a voltage equivalent to the amount it would rise in the time τ , which is:

$$\tau(dV/dt) = \tau(i/C) = \tau(iR/CR) \quad (14)$$

where we have not said what R is yet. However, CR is clearly a time constant, and if we make $CR = \tau$, we see that the correction voltage becomes just iR . Thus we can add this voltage simply by putting a resistor R in series with C , where $R = \tau/C$.

Usually the resistor R is small enough that the discharge switch can just be put across the R - C series without significantly effecting the final discharge level of C , or a second shorting switch can be used if necessary. Where only the output pulse is of interest (not the sawtooth), τ can be made artificially long to swamp other timing errors. [Such is the case with voltage-to-frequency converters where high conversion accuracy is desirable, but waveshape is not.] Addition of this correction voltage will cause some imperfections to appear in the output waveform, which are however not necessarily a problem. The method works the same way for a triangle wave generator.

▷ Choice of transistors used in these circuits is quite important. In general, the best matched monolithic pairs available should be used. The Analog Devices Inc. type AD818 is an excellent log conformance matched pair for NPN needs, while the AD821 from the same manufacturer is a good choice when PNP pairs are required. It is in general much easier to find NPN pairs than it is to find PNP pairs. Transistors on arrays are useful, such as the CA3046 NPN array, and the CA3084 PNP array. Selected matched individual transistors glued together are a possible choice for non-critical needs.

▷ REFERENCES:

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- B. Hutchins, "Design Procedures for Using Exponential Converters to Perform Mathematical Operations," Electronotes, Vol. 8, No. 69, Sept. 1976
- D. H. Sheingold (Ed) Nonlinear Circuits Handbook, Analog Devices Inc., Norwood, MA 02062 (about \$5.95)(1976)
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